IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. **RA043D2C6C2**)

In the Application of:

FARMWALD ET AL.

Serial No: Continuation of 09/629,497

Filed: Herewith

Title: MEMORY DEVICE HAVING A PROGRAMMABLE REGISTER (As Amended)

Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Dear Sir:

Prior to the examination of the above-referenced application, kindly amend the application as follows:

<u>IN THE ABSTRACT</u>:

Please delete the Abstract of the Disclosure and substitute the attached Abstract of the Disclosure.

<u>IN THE TITLE</u>:

Please delete the title and substitute --MEMORY DEVICE HAVING A PROGRAMMABLE REGISTER--.

IN THE SPECIFICATION:

On page 1, line 8, insert --This application is a continuation of Application No. 09/629,497, filed July 31, 2000 (pending); which is a continuation of Application No. 09/566,551, filed May 8, 2000 (pending); which is a continuation of Application No. 09/213,243, filed December 17, 1998 (now U.S. Patent 6,101,152); which is a continuation of Application No. 09/196,199, filed on November 20, 1998 (now U.S. Patent 6,038,195), which is a continuation of Application No. 08/798,520, filed on February 10, 1997 (now U.S. Patent 5,841,580); which is a division of Application No. 08/448,657, filed May 24, 1995 (now U.S. Patent 5,638,334); which is a division of Application No. 08/222,646, filed on March 31, 1994 (now U.S. Patent 5,513,327); which is a continuation of Application No. 07/954,945, filed on September 30, 1992 (now U.S. Patent 5,319,755); which is a continuation of Application No. 07/510,898, filed on April 18, 1990 (now abandoned).--

On page 3, line 9, delete "micro-processor" and substitute --microprocessor--.

On page 6, line 1, delete "4,646,279" and substitute --4,646,270--.

On page 10, line 18, delete "Figure 7 shows" and substitute --Figures 7a and 7b show--.

On page 10, line 21, delete "Figure 8 shows" and substitute --Figures 8a and 8b show--.

On page 11, line 14, insert:

--Figure 16 is a block diagram representation of a set of internal registers within each device illustrated in Figure 2.--

On page 14, line 3, replace "Each" with --With reference to Figure 16, each--.

On page 14, line 4, after "registers" insert --170--.

On page 14, line 5, after the **first** occurrence of "register" insert --171--.

On page 14, line 5, after the **second** occurrence of "register" insert --174--.

On page 14, line 6, after the **first** occurrence of "register" insert --175--.

On page 14, line 8, after "registers" insert --172--.

On page 14, line 10, after "registers" insert --173--.

On page 14, line 17, after "register" insert --171--.

On page 14, line 20, after the **first** occurrence of "registers" insert --173--.

On page 14, line 20, after the **second** occurrence of "registers" insert --175--.

On page 14, line 20, after the **third** occurrence of "registers" insert --172--.

On page 14, line 22, after "registers" insert --173--.

On page 21, line 15, after "registers" insert --173--.

On page 34, line 4, after "devices" insert --do--.

On page 35, line 25, after "registers" insert --170--.

On page 36, line 10, after "registers" insert --173--.

On page 36, line 15, after "register" insert --171--.

On page 36, line 12, after "registers" insert --172--.

On page 38, line 25, after "register" insert --173--.

On page 39, line 6, after "register" insert --173--.

On page 41, line 1, delete "or' "and substitute -- or--.

On page 45, line 17, delete "Fig. 7" and substitute --Figures 7a and 7b--.

On page 47, line 2, delete "Figure 8" and substitute --Figure 8a--.

On page 47, line 5, delete "from left to right" and substitute -- from right to left--.

On page 47, line 8, delete "right" and substitute --left--.

On page 47, line 9, delete the first "left" and substitute --right--.

On page 49, line 22, delete "primay" and substitute --primary--.

On page 54, line 13, delete "70" and substitute --69--.

On page 56, line 2, delete "Figurell" and substitute --Figure 11--.

On page 58, line 22, after "clocks" insert --73 and 74, respectively--.

On page 60, line 10, after "147" insert --A, B-.

IN THE CLAIMS:

Kindly **cancel** claims 1-150, without prejudice.

Kindly **add** the following claims:

--151. A method of operation of a synchronous memory device, wherein the memory device includes an array of memory cells and a programmable register, the method of operation of the memory device comprises:

sampling a first operation code synchronously with respect to a transition of an external clock signal;

receiving a binary value synchronously with respect to the external clock signal, wherein the binary value is representative of a delay time to transpire before the memory device is to output data in response to a second operation code, wherein the second operation code initiates a read operation in the memory device; and

storing the binary value in the programmable register in response to the first operation code.

152. The method of claim 151 wherein the first operation code is included in a control register access request packet.

153. The method of claim 152 wherein the first operation code and the binary value are included in the same control register access request packet.

154. The method of claim 151 wherein the delay time is representative of a number of clock cycles of the external clock signal to transpire.

155. The method of claim 154 further including:

receiving the second operation code; and

outputting the data, in response to the second operation code, after the number of clock cycles of the external clock signal transpire.

156. The method of claim 155 further including receiving address information synchronously with respect to the external clock signal.

157. The method of claim 156 wherein the address information and the second operation code are included in a read request packet.

158. The method of claim 151 further including:

receiving block size information wherein the block size information is representative of an amount of data to be output;

receiving the second operation code; and

outputting the amount of data in response to the second operation code, after delay time transpires.

159. The method of claim 158 wherein the block size information further defines an amount of data to be input in response to a third operation code, wherein the third operation code initiates a write operation in the memory device, the method further including:

receiving the third operation code; and

inputting the amount of data in response to the third operation code.

160. The method of claim 159 wherein the third operation code is included in a request packet.

161. The method of claim 160 wherein the block size information and the third operation code are included in the same request packet.

162. The method of claim 155 wherein data is output synchronously with respect to consecutive rising and falling edge transitions of the external clock signal.

163. The method of claim 151 wherein the first operation code is received in an initialization sequence after power is applied to the memory device.

164. A method of controlling a synchronous memory device by a controller, wherein the memory device includes an array of memory cells and a programmable register, the method of controlling the memory device comprises:

issuing a first operation code to the memory device, wherein the first operation code initiates an access of the programmable register in the memory device in order to store a binary value; and

providing the binary value to the memory device, wherein the memory device stores the binary value in the programmable register in response to the first operation code.

165. The method of claim 164 wherein the binary value is representative of a number of clock cycles of an external clock signal

to transpire before the memory device outputs data in response to a second operation code.

166. The method of claim 165 further including:

issuing the second operation code to the memory device; and

receiving data output by the memory device after the number of clock cycles of the external clock signal transpire.

167. The method of claim 166 further including providing address information synchronously with respect to the external clock signal.

168. The method of claim 167 wherein the address information and the second operation code are included in a request packet.

169. The method of claim 164 further including:

providing block size information to the memory device, wherein the block size information defines an amount of data to be output by the memory device in response to the second operation code; and

receiving the amount of data output by the memory device.

170. The method of claim 169 wherein the block size information further defines an amount of data to be input by the memory device in response to a third operation code, the method further including:

issuing the third operation code to the memory device; and

providing the amount of data to the memory device.

171. The method of claim 164 wherein the first operation code and the binary value are included in a request packet.

172. The method of claim 164 wherein the first operation code and the binary value are included in the same request packet.

173. A synchronous memory device including an array of memory cells and at least one programmable register, the synchronous memory device comprises:

clock receiver circuitry to receive an external clock signal;

input receiver circuitry to sample a first operation code synchronously with respect to a transition of the external clock signal; and

a programmable register to store a binary value, wherein the memory device stores the binary value in the programmable register in response to the first operation code.

174. The memory device of claim 173 wherein the binary value is representative of a number of clock cycles of the external clock signal to transpire before the memory device outputs data in response to a second operation code.

175. The memory device of claim 174 further including output driver circuitry to output the data after the number of clock cycles of the external clock signal transpire in response to the second operation code.

176. The memory device of claim 175 wherein the output driver circuitry outputs a first portion of data synchronously with respect to a rising edge transition of the external clock signal and a second portion of data synchronously with respect to a falling edge transition of the external clock signal.

177. The memory device of claim 173 wherein the first operation code is included in a request packet.

178. The memory device of claim 173 wherein the first operation code and the binary value are included in a request packet.

179. The memory device of claim 173 wherein the first operation code and the binary value are included in the same request packet.

180. The memory device of claim 173 wherein the input receiver circuitry is operative to receive a third operation code, wherein the third operation code initiates a write operation in the memory device, and wherein the memory device further includes:

input circuitry to input data in response to the third operation code.--

REMARKS

This Preliminary Amendment seeks to place this application in condition for allowance. This application is a continuation of Application No. 09/629,497 which is a continuation of Application No. 09/566,551. Application Serial No. 09/629,497 is pending.

REQUEST FOR PRIORITY

Applicants request priority to Application Serial No. 07/510,898, filed April 18, 1990, now abandoned. Applicants request such priority through Application No. 09/629,497 (pending), filed July 31, 2000; which is a continuation of Application No. 09/566,551 filed on May 8, 2000 (pending); which is a continuation of Application No. 09/213,243, filed December 17, 1998 (now U.S. Patent 6,101,152)(now U.S. Patent 6,034,918); which is a continuation of Application No. 09/196,199, filed on November 20, 1998 (now U.S. Patent 6,038,195), which is a continuation of Application No. 08/798,520, filed on February 10, 1997 (now U.S. Patent 5,841,580); which is a division of Application No. 08/448,657, filed May 24, 1995 (now U.S. Patent 5,638,334); which is a division of Application No. 08/222,646, filed on March 31, 1994 (now U.S. Patent 5,513,327); which is a continuation of Application No. 07/954,945, filed on September 30, 1992 (now U.S. Patent 5,319,755); which is a continuation of Application No. 07/510,898, filed on April 18, 1990 (now abandoned).

Accordingly, Applicants claim the benefit of the filing date of Application Serial No. 07/510,898 -- i.e., April 18, 1990. The specification has been amended to identify the continuation or related U.S. application data identified above. No new matter has been added.

AMENDMENTS TO THE CLAIMS

In this continuation application, Applicants present new claims which set forth novel and unobvious features of Applicants' invention. Applicants submit new claims 151-180 to more fully protect the Applicants invention. No new matter has been added.

The newly submitted claims are believed to be fully supported by the specification -- see, for example, Figures 2, 4, and 10-13; page 14, line 3 to page 16, line 7; page 20, line 14 to page 21, line 20; page 22, line 11 to page 25, line 8; page 27, line 1 to page 28, line 20; page 46, line 19 to page 48, line 17; page 53, line 23 to page 55, line 19; page 71, line 14 to page 72, line 21;and page 115, lines 10-22.

AMENDMENTS TO THE SPECIFICATION

Applicants have also amended the specification to include the priority data, reflect changes to the drawings and to correct obvious spelling, typographical and grammatical errors. No new matter has been added.

AMENDMENTS TO THE ABSTRACT

A new Abstract of the Disclosure is attached hereto. No new matter has been added.

DRAWING CHANGES

Accompanying this Preliminary Amendment is a Request to Approve Drawing Changes. Applicants have amended the drawings to show every feature of the invention specified in the claims. To that end,

Applicants submit herewith new Figure 16. A copy of Applicants Request to Approve Drawing Changes is attached.

New Figure 16 is added to illustrate, among other things, access-time register(s) 173. Figure 16 illustrates one embodiment of the internal registers within each device illustrated in Figure 2. Support may be found in the specification at page 14, lines 3-21 and page 53 lines 4-21. No new matter has been added.

Applicants seek to amend Figure 10 to more fully reflect the discussion in the specification, in particular, page 55, lines 12-16 and page 58, lines 13-23. The proposed changes are indicated in red. No new matter has been added. Applicants respectfully request that the Examiner approve the proposed changes to Figure 10. A new Figure 10 which incorporates the changes is also attached to the Request.

CONCLUSION

Applicants request entry of the foregoing amendment prior to examination of this application. Applicants submit that all of the claims present patentable subject matter. Accordingly, Applicants respectfully request allowance of all of the claims.

Respectfully submitted,

Date: March 6, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

ABSTRACT OF THE DISCLOSURE

A synchronous memory device and methods of operation and controlling such a device. The synchronous memory device includes clock receiver circuitry to receive an external clock signal and input receiver circuitry to sample a first operation code synchronously with respect to a transition of the external clock signal. The synchronous memory device also includes a programmable register to store a binary value, wherein the memory device stores the binary value in the programmable register in response to the first operation code.

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Assistant Commissioner for Patents
Washington, DC 20231

REQUEST TO APPROVE DRAWING CHANGES

Dear Sir:

Attached hereto is new Figure 16. Figure 16 illustrates the internal registers which reside in each device illustrated in Figure 2. This embodiment is described in the specification at page 14, lines 3-21 and page 53 lines 4-21. No new matter has been added.

Applicants seek to amend Figure 10 to more fully reflect the discussion in the specification, specifically, page 55, line 12-16 and page 58, lines 13-23. Also attached, is a photocopy of Figure 10 with the proposed changes indicated in red. No new matter has been added.

Applicants respectfully request that the proposed new Figure 16 be approved by the Examiner. Applicants also respectfully request approval of the proposed changes to Figure 10. A new Figure 10 which incorporates the changes is also attached hereto.

Respectfully submitted,

Date: March 6, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

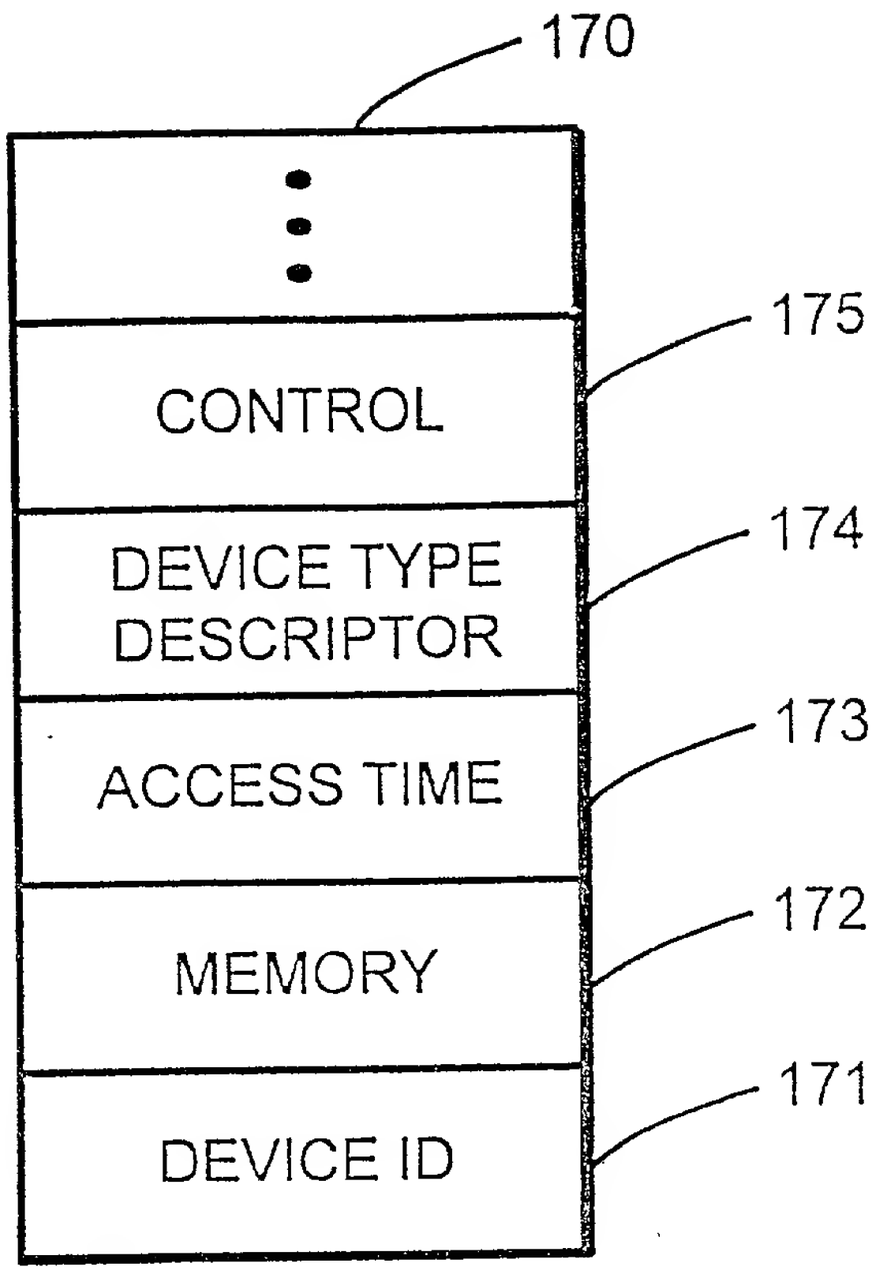
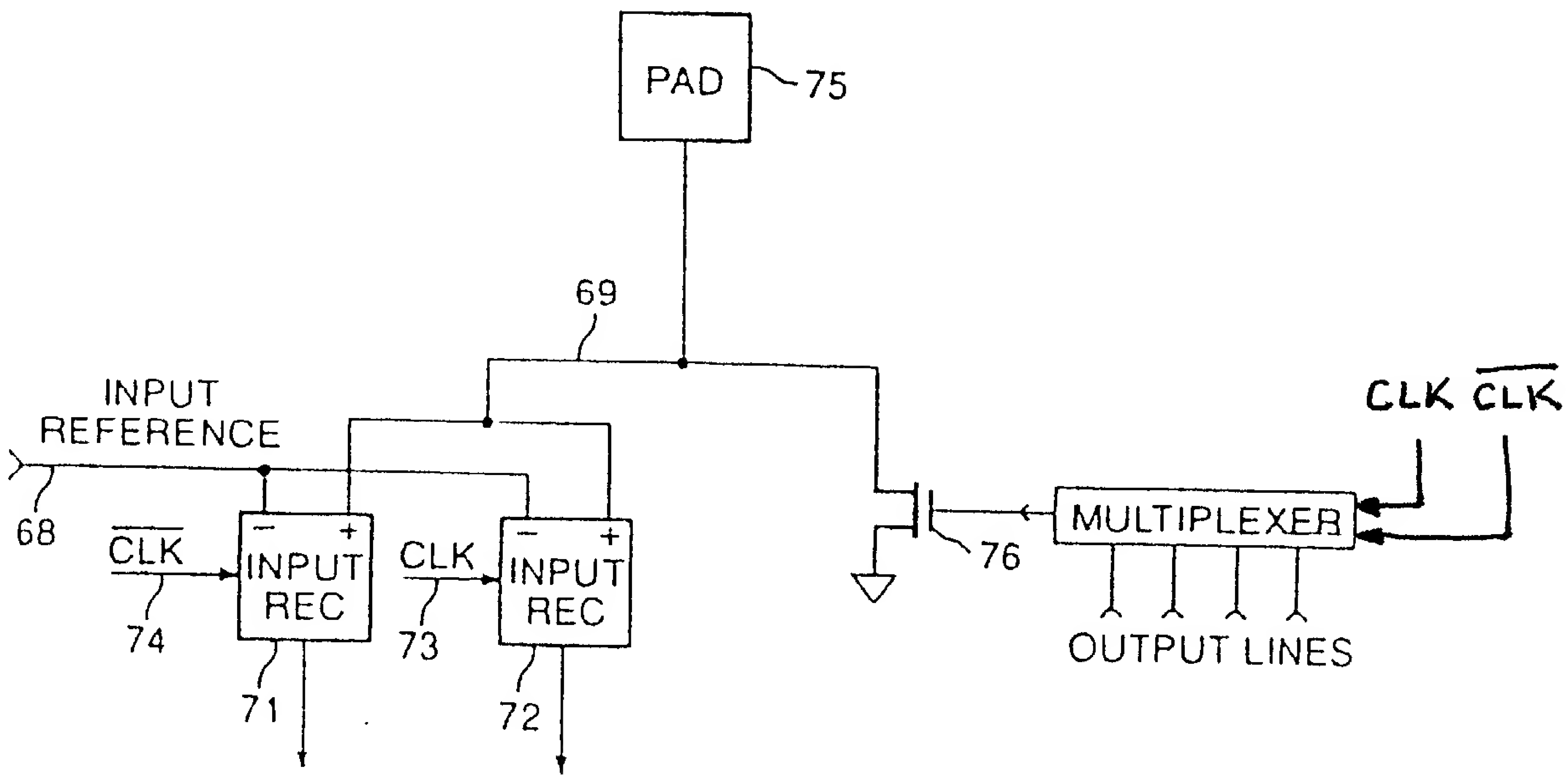

170
175
CONTROL
174
DEVICE TYPE DESCRIPTOR
173
ACCESS TIME
172
MEMORY
171
DEVICE ID

FIG. 16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REC
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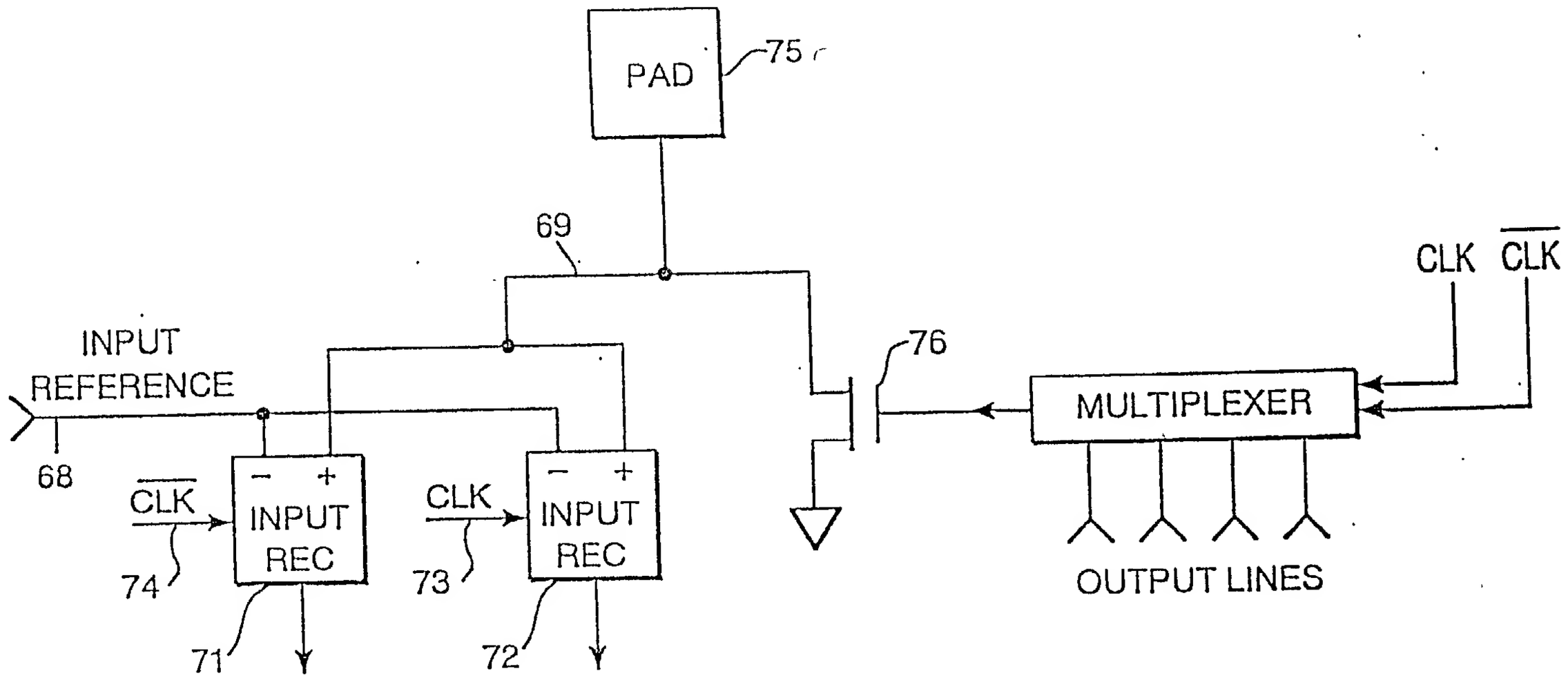
MULTIPLEXER
OUTPUT LINES
CLK CLK

FIG. 10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MULTIPLEXER
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74
INPUT
REC
CLK
73
INPUT
REC
71
72
OUTPUT LINES

FIG 10